Claim Listing

Please cancel claims 1-19.

Please add the following new claims:

20. (New) A method for reducing electrical power dissipation in a computer system, comprising:

providing:

a counter corresponding to a data channel;

a processor coupled to receive computer program instructions and configured to execute the received computer program instructions;

determining at least one component of the processor that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions;

decrementing a count stored in the counter when the processor executes an instruction corresponding to the data channel; and

transitioning the at least one component of the processor to a low power mode in the event the count stored in the counter reaches a predetermined value.

21. (New) The method as recited in claim 20, wherein the transitioning comprises:

transitioning the at least one component of the processor to a low power mode in the event the count stored in the counter reaches either: (i) a predetermined minimum value corresponding to a predetermined minimum amount of data in the data channel, or (ii) a predetermined maximum value corresponding to a predetermined maximum amount of data in the data channel.

22. (New) A computer system, comprising:

a counter corresponding to a data channel;

a processor coupled to receive computer program instructions and a power control signal, wherein the processor is configured to execute the received computer program instructions, and wherein the processor comprises at least one component that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions, and wherein the processor is configured to transition the at least one component to a low power mode in response to the power control signal;

means for decrementing a count stored in the counter when the processor executes an instruction corresponding to the data channel; and

means for producing the power control signal in the event the count stored in the counter reaches a predetermined value.

23. (New) The computer system as recited in claim 22, wherein the computer system comprises a channel unit, and wherein the channel unit comprises the counter, and wherein the channel unit is configured to decrement the count stored in the counter when the processor executes an instruction corresponding to the data channel.

24. (New) The computer system as recited in claim 23, wherein the processor is configured to provide a signal to the channel unit in the even an instruction corresponding to the data channel is executed, and wherein the channel unit is configured to produce a wait signal in the event the count stored in the counter reaches the predetermined value.

25. (New) The computer system as recited in claim 24, further comprising an instruction issue unit coupled to receive computer program instructions and the wait signal produced by the channel unit, wherein the instruction issue unit is configured to provide the computer program instructions to the processor and to respond to the wait signal by producing the power control signal.

26. (New) A computer system, comprising:

a channel unit coupled to receive an external channel event signal corresponding to a data channel, wherein the channel unit comprises a counter corresponding to the data channel, and wherein the channel unit is configured to produce a wait signal;

an instruction issue unit coupled to receive computer program instructions and the wait signal produced by the channel unit, wherein the instruction issue unit is configured to provide the computer program instructions and to produce a power control signal;

a processor coupled to the channel unit and to receive the computer program instructions and the power control signal from the instruction issue unit, wherein the processor is configured to execute the received computer program instructions;

wherein the processor is configured to provide a signal to the channel unit in the even an instruction corresponding to the data channel is executed;

wherein the channel unit is configured to respond to the signal from the processor by decrementing a count stored in the counter, and to produce the wait signal in the even the count reaches a predetermined value;

wherein the instruction issue unit is configured to respond to the wait signal by producing the power control signal;

wherein the processor comprises at least one component that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions; and

wherein the processor is configured to respond to the power control signal from the instruction issue unit by transitioning the at least one component to a low power mode.

27. (New) The computer system as recited in claim 26, wherein the channel unit is configured to produce the wait signal in the even the count stored in the counter is a predetermined minimum value corresponding to a predetermined minimum amount of data in the data channel.

28. (New) The computer system as recited in claim 26, wherein the channel unit is configured to produce the wait signal in the even the count stored in the counter is a predetermined maximum value corresponding to a predetermined maximum amount of data in the data channel.

29. (New) The computer system as recited in claim 26, wherein the at least one component that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions comprises a fixed point math unit, a branch unit, an instruction decode unit, an instruction storage unit, a load/store unit, or a floating point math unit.

30. (New) The computer system as recited in claim 26, wherein the channel unit is configured to respond to the external channel event signal by incrementing the count stored in the counter.

31. (New) A computer system, comprising:

a channel unit coupled to receive an external channel event signal corresponding to a blocking channel of a plurality of data channels, and wherein the channel unit comprises a plurality of counters each corresponding to a different one of the data channels, and wherein the channel unit is configured to produce a wait signal;

an instruction issue unit coupled to receive computer program instructions of an instruction set and the wait signal produced by the channel unit, wherein the instruction issue unit is configured to provide the computer program instructions and to produce a power control signal;

a processor coupled to the channel unit and to receive the computer program instructions and the power control signal from the instruction issue unit, wherein the processor is configured to execute the received computer program instructions;

wherein the processor is configured to provide a signal to the channel unit in the even an instruction corresponding to one of the data channels is executed;

wherein the channel unit is configured to respond to the signal from the processor by decrementing a count stored in the counter corresponding to the data channel, and to produce the wait signal in the even the count corresponding to the blocking channel is a predetermined value;

wherein the instruction issue unit is configured to respond to the wait signal by producing the power control signal;

wherein the processor comprises at least one component that is not used when the processor has executed all received computer program instructions and is waiting for further computer program instructions; and

wherein the processor is configured to respond to the power control signal from the instruction issue unit by transitioning the at least one component to a low power mode.

32. (New) The computer system as recited in claim 31, wherein each of the data channels is assigned a different channel number, and wherein each of the computer program instructions corresponds to one of the data channels and comprises the channel number of the corresponding data channel.

33. (New) The computer system as recited in claim 31, wherein the signal provided by the processor to the channel unit when a computer program instruction is executed comprises the channel number of the corresponding data channel.

34. (New) The computer system as recited in claim 33, wherein the channel unit is configured to respond to the signal from the processor by decrementing the count stored in the counter corresponding to the data channel having the channel number.

35. (New) The computer system as recited in claim 31, wherein the channel unit is configured to produce the wait signal in the even the count stored in the counter corresponding to the blocking channel is a predetermined minimum value corresponding to a predetermined minimum amount of data in the blocking channel.

36. (New) The computer system as recited in claim 31, wherein the channel unit is configured to produce the wait signal in the even the count stored in the counter corresponding to the blocking channel is a predetermined maximum value corresponding to a predetermined maximum amount of data in the blocking channel.

37. (New) The computer system as recited in claim 31, wherein the channel unit is configured to respond to the external channel event signal by incrementing the count stored in the counter corresponding to the blocking channel.

38. (New) The computer system as recited in claim 31, wherein the instruction set comprises a channel read operation instruction, and wherein the channel read operation instruction comprises a channel number and identifies a register of the processor where data of the data channel having the channel number is to be stored.

39. The computer system as recited in claim 31, wherein the instruction set comprises a channel write operation instruction, and wherein the channel write operation instruction comprises a channel number and identifies a register of the processor where data of the data channel having the channel number is to be obtained.